REMARKS

Reconsideration and allowance of this application are respectfully requested. Claims 1, 6-9 and 15-17 have been amended. Claim 20 has been canceled. Claims 1-19 are now pending in the application. The rejections are respectfully submitted to be obviated in view of the amendments and remarks presented herein.

Claim Objections

Claims 12 and 13 have been objected to because of alleged informalities. However, Applicant believes that the recitation of "said delaying and adding" in claim 12 is a proper reference to "delaying and adding signals" as recited in claim 10. The signals as referred to are delayed and added, thus the word "said" in line 4 of claim 12 is believed to be properly referencing the delaying and adding as recited in claim 10. Therefore, Applicant respectfully requests withdrawal of the objection to claims 12 and 13.

Rejection Under 35 U.S.C. § 112, First Paragraph

Claims 5 and 13 have been rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement. The rejection is respectfully traversed.

Regarding claim 5, Applicant recites that "said adders input said received quality during the current symbol to be demodulated by using a feedback circuit." This is clearly shown in FIG. 1. Adders such as one of adders 6, 8, 23 and 24 are claimed to obtain phase differences for symbols before and after the current symbol to be demodulated, as recited in claim 3. Outputs from these adders are also used by operation circuits such as one of operation circuits 9, 11, 25 and 26 to obtain a received quality, as recited in claim 4. Claim 5 recites, further, that the adders

input the received quality by using a feedback circuit. This is clearly shown in FIG. 2, whereby each of adders 6-8, 23, 24 and 33 receive a feedback signal which has been weighted by W3 (37). Therefore, the input of reception quality by the adders is another feature of Applicant's claimed invention, an exemplary embodiment of which is shown in FIG. 1. Claim 13 recites a similar feature, and is allowable for analogous reasons. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 112, first paragraph, are respectfully requested.

Rejection Under 35 U.S.C. § 112, Second Paragraph

Claims 1-16 have been rejected under 35 U.S.C. § 112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. In response, claims 1, 6-9, 15 and 16 have been editorially amended. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 112, second paragraph, are respectfully requested.

Rejection Under 35 U.S.C. § 103(a) - Yanagi et al. in view of Adachi

Claims 17-19 have been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yanagi et al. (U.S. Patent Number 5,528,627; hereinafter "Yanagi") in view of Adachi (U.S. Patent Number 5,654,667). The rejection is respectfully traversed.

As a preliminary matter, Applicant notes that the Examiner has indicated claim 19 to be rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yanagi in view of Adachi, however, Applicant believes that the Examiner only intended to reject claims 17, 18 and 20 under this combination of references.

Regarding claim 17, as amended, Applicant's claimed invention is a demodulator for demodulating digital symbol data, comprising a first weighting circuit, a detecting circuit, and a second weighting circuit. An output of the detecting circuit is input to an external circuit which generates correction values to which the first weighting circuit applies respective first weighting factors. The second weighting circuit applies respective second weighting factors to a difference between a current symbol and a delayed symbol detected and outputted by the detecting circuit.

Turning to the cited art, Yanagi describes a signal reception system as shown in FIG. 2. A reception signal at input terminal (15) is demodulated by demodulation circuit (11) to generate a demodulated signal (column 3, lines 44-47). An adaptive filter (12) with a plurality of taps as shown in FIG. 3 produces a filtered signal. An error signal control circuit (20) passes an error signal generated by error signal generation circuit (14) when a first delayed signal received from a 1st delay circuit (13-1) is greater than a threshold value (column 4, lines 15-29). A differential detection circuit (13) generates a synchronized signal synchronized with the phase of the carrier wave by performing a differential detection operation, through integrating the filtered signal and the filtered signal delayed by the 1st delay circuit (13-1), by integrating circuit (13-2).

The Examiner maintains that the combination of Yanagi and Adachi teaches each feature of the claimed invention. However, in Yanagi, the error signal control circuit (20) does not generate a correction value. The error signal control circuit only passes the error signal from error signal generation circuit (14) when the 1st delayed signal is greater than a threshold value (column 4, lines 15-29). Additionally, the error signal control circuit (20) cannot even be considered to be an "external" circuit, as claimed, because the error signal control circuit (20) is

necessary and essential for the function of controlling the adaptive filter (12), and is also considered to be part of a weighting circuitry when taken together with the adaptive filter. Applicant's claimed invention recites "a first weighting circuit that applies respective first weighting factors to one or more correction values generated by an external circuit." If the output from Yanagi's error signal control circuit (20) is considered to be correction values, then the adaptive filter (12) is required to apply first weighting factors to error signal from the error signal control circuit (20). This is clearly not occurring in Yanagi. Instead, the error signal is merely used to control the taps to multiply the demodulated signal from demodulation circuit (11) with coefficients. The signal reception as shown in FIG. 2 does not apply first weighting factors to correction values generated by an external circuit, as Applicant claims. Furthermore, the demodulated signal also can not be interpreted as correction values as Applicant has claimed. Applicant's claim 17 recites that "the external circuit receives as an input the output of said detecting circuit." Yanagi does not teach or suggest such an external circuit, and the error signal control circuit (20) can not function similarly. The feedback in Yanagi only supplies the error signal to control the coefficients of the adaptive filter (12), and can not be considered to be correction values as claimed.

Adachi does not remedy the deficiencies of Yanagi. Adachi teaches a differential detector as shown in FIG. 3, in which a multiplier (P25) multiples a signal from subtractor (P23) with a complex conjugate from transformation part (P24). However, this circuitry operates only to implement Adachi's equation 9 on column 7, line 35. It is a complex conjugate which is multiplied by multiplier (P25) with the subtraction result from subtractor (P23). Furthermore,

the subtractor (P23) only obtains a subtraction result of a delayed signal sample z_{n-1} multiplied by a complex form of a phase $\Delta\varphi_n$ set in the Viterbi decoding part (17), from a received signal sample z_n (column 8, lines 9-35). The subtraction performed in subtractor (P23) is not "a difference between a current symbol and a delayed symbol," and the complex conjugate is not "second weighting factors," as Applicant claims. Additionally, Adachi also does not teach an external circuit generating correction values to which a first weighting circuit applies respective first weighting factors, as Applicant also claims. At least by virtue of the aforementioned differences, the invention defined by Applicant's claim 17 is patentable over Yanagi in view of Adachi. Applicant's claims 18 and 19 are dependent claims including all of the elements of independent claim 17, which, as established above, distinguishes over Yanagi in view of Adachi. Therefore, claims 18 and 19 are distinguished over Yanagi in view of Adachi for at least the aforementioned reasons as well as for their additionally recited features. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are respectfully requested.

With further regard to claim 18, a deciding circuit is described which determines an order of priority for the one or more weighted correction values. There is no mention in FIG. 3 from either Yanagi or Adachi that an order or priority is determined. At least by virtue of this additional difference as well as the aforementioned differences, Applicant's claimed invention distinguishes over Yanagi in view of Adachi.

Rejection Under 35 U.S.C. § 103(a) - Yanagi et al. in view of Adachi and further in view of Tsumura

Claim 19 has been rejected under 35 U.S.C. § 103(a) as allegedly being unpatentable over Yanagi in view of Adachi and further in view of Tsumura (U.S. Patent Number 5,511,097). The rejection is respectfully traversed.

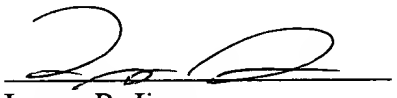
Yanagi in view of Adachi does not teach or suggest Applicant's invention as recited in claim 17, as discussed above. Tsumura does not remedy the deficiencies of Yanagi in view of Adachi. Tsumura describes only a delay detection circuit as shown in FIG. 1, in which a phase difference signal (107) is fed back to first and second phase compensation quantity estimators (5a and 5b). There is also no teaching or suggestion in Tsumura of an external circuit generating correction values to which a first weighting circuit applies respective first weighting factors, and wherein the external circuit receives as an input the output of a detecting circuit, as Applicant claims. Applicant's claim 19 is a dependent claim including all of the elements of independent claim 17, which, as established above, distinguishes over Yanagi in view of Adachi and further in view of Tsumura. At least by virtue of the aforementioned differences as well as for its additionally recited features, the invention defined by Applicant's claim 19 is patentable over Yanagi in view of Adachi and further in view of Tsumura. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) are respectfully requested.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the

Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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